ESDI Fixed Disk Drive Adapter/A Technical Reference

ESDI Fixed Disk Drive Adapter/A

6280015

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Description

The ESDI Fixed Disk Drive Adapter/A supports two Enhanced Small Device Interface (ESDI) type devices. The adapter is designed to work in systems that use the Micro Channel™ architecture. For more information about the architecture, refer to the system *Technical Reference* manual.

Both direct memory access (DMA) and programmed input/output (PIO) data transfers between the attached devices, adapter and system are supported.

Features

The adapter has the following features:

- Logical block and physical sector size of 512 bytes
- Multiple block data transfer, up to 64K (K = 1024) blocks
- Relative byte address (RBA) and absolute byte address (ABA) architecture
- Error detection and correction:
  - ID fields on disk—4 byte error-checking and correction (ECC) code (detection only)
  - Data fields on disk—4 byte ECC code
- Data transfer rate—up to 10 Mbps (million bits per second), non-return-to zero (NRZ)
- Multitasking—command queues for all attached devices.
- On-board ROM for BIOS; supports interrupt sharing.
- ROM-resident diagnostics.

The adapter provides the proper sequence and timing of signals to each attached device to position the access mechanism, enable and

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clock the data path, and transfer the data through the working buffer to its destination. Data is transferred to and from the adapter by DMA. The adapter provides an error recovery procedure, which includes:

- Re-reads at off-track locations
- Shifted data strobes
- ECC mechanism.

Direct Memory Access Requests

DMA requests from the adapter are enabled or disabled by programming the Basic Control register.

To support multiple data transfer commands the system must keep adapter DMA requests disabled between data transfers. The adapter interrupts when it is ready for data transfers to begin. (An outstanding data transfer command is determined by examining the device select code in the Interrupt Status register.) The system:

1. Sets its DMA controller appropriately for the pending data transfer
2. Enables the adapter DMA request capability.

Logic on the adapter disables DMA requests upon detecting the terminal count condition at the end of a data transfer operation.

Recording Format

Each track on a device is partitioned into sectors. The sector boundaries are defined by device sector or index pulses and are 512 bytes of data and various control information. Each sector is divided into an ID field and a data field. The format of a sector is as follows:

Number of Bytes	Data	Function
x	Hex 00	PLO Sync (Device Specification)
1	Hex A1	ID Sync
4	RBA	LSB - MSB
1	IDDC	Flag/Defect Count
4	ECC	ID Error Correction Code
4	Hex 00	PAD
1	Hex 00	Write Splice
x	Hex 00	PLO Sync (Device Specification)
1	Hex A1	Data Sync
512	DATA	User Data
4	ECC	Data Error Correction Code
2	Hex 00	PAD
y	ISG	Inter-Sector Gap (Device Specification)

Figure 1. Sector Format

Note: In the table above, x and y are determined by the device specification.

Phase Locked Oscillator Sync Fields

The adapter obtains phase locked oscillator (PLO) sync fields lengths by reading the device configuration using the Request Specific Configuration command.

Relative Byte Address (RBA)

The relative byte address consists of 28 bits contained in 4 bytes (32 bits). The relative byte address field is stored in the ID with the least significant bit (LSB) first and the most significant bit (MSB) last. The remaining 4 bits are used to identify certain sector characteristics as shown in the following figure:

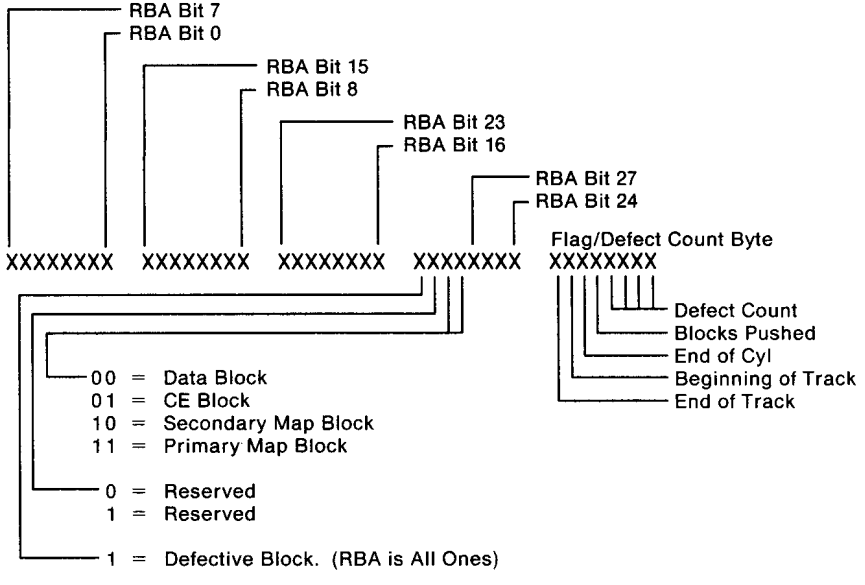


Figure 2. Relative Byte Address (RBA)

Flag/Defect Count Byte

The contents of the Flag/Defect Count byte shown in Figure 2 on page 4 are indicated in the following figure:

Bit	Name
7	End of Track
6	Beginning of Track
5	End of Cylinder
4	Blocks Pushed
3 - 0	Defect Count

Figure 3. Flag/Defect Count Byte

7 This bit is set to 1 if the block is the last logical block on the track.

6 This bit is set to 1 if the block is the first logical block on the track.

5 This bit is set to 1 if the block is in the last logical block on the cylinder.

4 This bit is set to 1 if one or more of the logical blocks on the track have been pushed to the next track.

3 - 0 Each ID on a given physical track contains the same defect count value. This value represents the number of blocks pushed onto this cylinder from the previous cylinder due to a higher number of defects on earlier cylinders than could not be contained locally on those cylinders. This localized defect area deficit problem is solved by borrowing defect areas from subsequent cylinders until defect management can catch up. To avoid seeks to the wrong cylinder, the adapter keeps track of this borrowing in a table. This table is read during power-on-reset.

Error-Checking and Correction (ECC)

The adapter provides ECC coding for both data and ID fields. This code has the capability to:

- Correct one 8-bit burst error with a miscorrection probability of 1 in 10^5

- Detect any two single bit errors (outside the 14-bit burst detection span)
- Detect any burst of errors within the 14-bit detection span (based on 512 byte blocks).

In the ID Field, ECC only detects errors; it does not to correct them.

Inter-Sector Gap (ISG)

The ISG begins immediately after the data pad and continues until the next Index or Sector pulse. It is therefore not of fixed length, but may vary slightly due to rotational speed tolerances.

Command Processing

The system requests the adapter to perform operations or commands. The flowcharts on the following pages show the basic flow required to process these commands.

The following notes are referred to in the flowcharts:

Notes:

1. The system BIOS times out if bit 4 in the Basic Status register is not set to 0 within four seconds, unless an Abort or Reset command is in progress.
2. During the transfer of the command block to the adapter, the system BIOS times out if the command word is not accepted by the adapter within 1 second.

The following are flowcharts for processing a command:

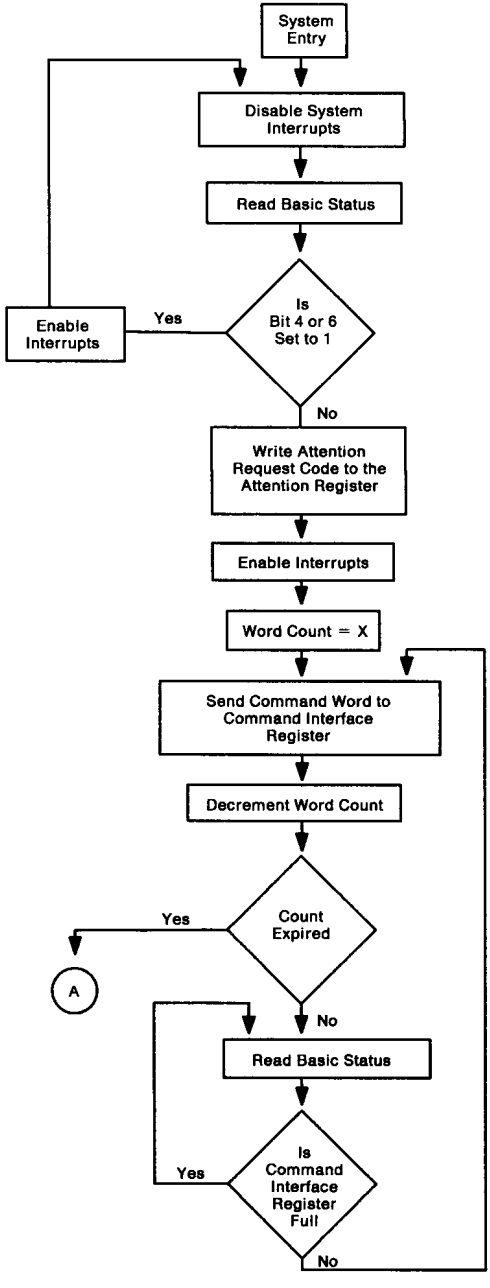


Figure 4. Processing a Command (Part 1 of 2)

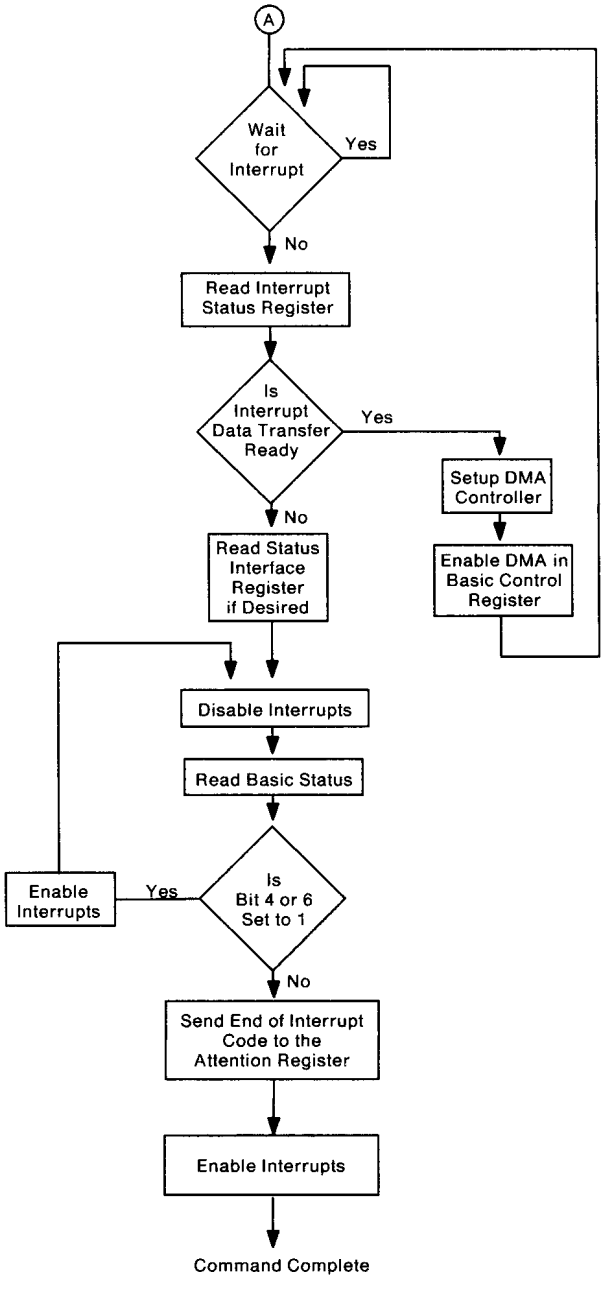


Figure 5. Processing a Command (Part 2 of 2)

Programmable Option Select (POS)

Before the adapter can be used, it must be initialized by the system. The POS registers eliminate the need to manually initialize the adapter for a particular configuration.

The adapter contains several configurable options. These options are controlled by the POS registers. The system can request POS information from the adapter with the Read POS Information command.

Warning: IBM recommends that programmable options be set only through the System Configuration Utilities. Direct setting of the POS registers and/or CMOS RAM POS parameters can result in multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the system or options. If application programs use adapter identification (ID) information, compatibility problems between systems or options may result.

The POS registers are only accessible by the system when -CD SETUP on the channel is active. Address lines A0 through A2 on the channel access these registers as shown in the following figure:

-CD SETUP	Address Lines A2 A1 A0	Register
L	L L L	POS Register 0 - Adapter ID
L	L L H	POS Register 1 - Adapter ID
L	L H L	POS Register 2 - Option Select
L	L H H	POS Register 3 - Option Select
H	X X X	Normal Operation

Figure 6. POS Registers

POS Registers 0 and 1

These read-only registers contain the hard-wired adapter ID.

When -CD SETUP is active, the hard-wired adapter ID (hex DDFF) is read by the system. POS Register 1 is the most-significant byte and POS Register 0 is the least-significant byte of the adapter ID.

POS Register 2

Programmable adapter options are written to this read/write register. Bit definitions for POS register 2 are shown in the following figure:

Bit	Function
7	Reserved = 0
6	Arbitration Method
5 - 2	Arbitration Level
1	Alternate Address
0	Adapter Enable

Figure 7. POS Register 2

Note: All bits in POS Register 2 are cleared to 0 during power-on.

Bit 7 Reserved, this bit is always cleared to 0.

Bit 6 When this bit is set to 1, fairness is disabled and priority is linearly assigned. When this bit is cleared to 0, fairness is enabled.

If the adapter is bursting data on the channel and -PREEMPT is active, the adapter stops channel activity and enters an inactive state. The adapter waits for -PREEMPT to become active before reentering arbitration.

Bits 5 - 2 These bits specify the arbitration priority level for the adapter. The highest priority is selected with the binary decode of 0000. When competing for the channel, the adapter places this value on the ARB lines. If no other device places a higher priority request (lower binary value) on these lines, the adapter wins the arbitration.

Bit 1 When this bit is set to 1, the adapter responds to addresses hex 3518 - 3151F. When this bit is set to 0, the adapter responds to addresses hex 3510 - 3517.

Bit 0 When this bit is set to 1, the adapter is enabled. When this bit is cleared to 0, the adapter is disabled. When disabled, the adapter will not respond to any I/O or Memory commands except the Memory Refresh command or POS reads and writes. No interrupt requests will be driven. A 'channel reset' clears this bit to 0.

POS Register 3

Programmable adapter options are written to this read/write register. Bit definitions for POS register 3 are shown in the following figure:

Bit	Function
7 - 6	Reserved = 0
5 - 4	Burst Length
3	ROM Disable
2 - 0	ROM Segment

Figure 8. POS Register 3

Bits 7 - 6 Reserved, these bits are always cleared to 0.

Bits 5 - 4 These bits indicate the Burst Length as shown in the following figure:

Bits 5 4	Function
0 0	Burst Disable
0 1	8-Word Bursts
1 0	16-Word Bursts
1 1	24-Word Bursts

Figure 9. Burst Length

Bit 3 When this bit is set to 1, ROM is disabled. When this bit is set to 0, ROM is enabled.

Bits 2 - 0 These bits are the ROM Segment decode. They are decoded as shown in the following figure:

Bits 2 1 0	Segment Address Hex
0 0 0	C0000 - C3FFF
0 0 1	C4000 - C7FFF
0 1 0	C8000 - CBFFF
0 1 1	CC000 - CFFFF
1 0 0	D0000 - D3FFF
1 0 1	D4000 - D7FFF
1 1 0	D8000 - DBFFF
1 1 1	DC000 - DFFFF

Figure 10. ROM Segment Decode

Adapter to System Interface

Once the POS registers have been read from or written to by the system, an interface of accessible command and status registers passes commands and receives status from the adapter.
The following figure provides a listing of the accessible registers:

Register Selected	Hex Address Primary/Alternate	Read/Write	Number of Bits
Attention	3513/351B	Write	8-bit
Basic Control	3512/351A	Write	8-bit
Basic Status	3512/351A	Read	8-bit
Interrupt Status	3513/351B	Read	8-bit
Command Interface	3510/3518	Write	16-bit
Status Interface	3510/3518	Read	16-bit

Figure 11. Accessible Registers

Attention Register

This 8-bit register requests the adapter to perform some function for the system. It remains set until loaded again. The bits in the register indicate the requested action and associated device number.

The system (with its interrupts disabled) reads the Basic Status register and verifies that bits 4 and 6 in the Basic Status register are cleared to 0 immediately before writing an attention request code to the Attention register.

When the system writes to the Attention register, bit 4 in the Basic Status register is immediately set to 1. A command block is then transferred to the adapter. Bit 4 in the Basic Status register remains set to 1 until the adapter is ready for another attention request code.

Attention register bit definitions are shown in the following figure:

Bit	Name
7 - 5	Device Select Code
4	Reserved = 0
3 - 0	Attention Request Code

Figure 12. Attention Register

Bits 7 - 5 These bits select the device: device 0, device 1, or the adapter. Device Select Codes are shown in Figure 13.

Note: Commands issued for a device not supported by the adapter are rejected with the status block indicating an invalid parameter in the command block.

Bits 7 6 5	Device Selected
0 0 0	Device 0
0 0 1	Device 1
0 1 0	Reserved
0 1 1	Reserved
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Adapter Command

Figure 13. Device Select Codes

Bit 4 This bit is reserved. It should always be cleared to 0.

Bits 3 - 0 The attention request code tells the adapter to perform a specific action for the device selected, as shown in the following figure:

Bits 3 2 1 0	Request Code
0 0 0 1	Command Request
0 0 1 0	End of Interrupt
0 0 1 1	Abort Command
0 1 0 0	Reset Adapter

Figure 14. Attention Request Codes

Command Request: This code requests the adapter to accept a command block from the system. The system can write to the Attention register and request additional commands during data transfers from a previous command. A maximum of three commands can be outstanding, one for each attached device and one global adapter command. If a command is directed to a busy device, the command is rejected and an an Attention Error is shown in the command status block.

When the requested command is complete, an interrupt is generated.

Note: No interrupts are issued by the adapter while command transfers are in progress.

When a request is complete, the Interrupt Status register is set to identify the completed request and completed condition. The Status Interface register also contains the first word of the Command Complete status block, if the word is available.

End-of-Interrupt: After an attention request code, an End-of-Interrupt attention request code must be written to the Attention register by the system before any further interrupts are issued or any changes are made to the Interrupt Status register.

If the system issues the End-of-Interrupt request before reading all of the sense summary block, the adapter interprets this as meaning that the system does not desire to read the rest of the sense block at this time and that the system is ready to accept another interrupt.

Abort Command: This request is only issued when the system has timed out while waiting for the Command Complete interrupt. When issued, this request stops the command in progress and maintains sense data for the command. This sense data is useful in determining what caused the command to time out. When the Abort Command request is complete, an interrupt is issued.

Note: A completed Abort Command request includes writing the Abort Complete status to the Interrupt Status register and writing the first word of the Command Complete status block for the aborted command.

Reset Adapter: This code causes the adapter to stop any activity with attached devices and perform an adapter reset that runs adapter diagnostics. This reset is equivalent to the power-on sequence.

During the reset, a recalibrate operation is performed on attached devices and configuration information is read from the devices. The Interrupt Status register indicates the result of the reset and an interrupt is generated when the reset is complete. Bit 4 in the Basic Status register is set to 1 during reset. A Reset complete interrupt is issued before the devices have finished recalibration.

Basic Control Register

This 8-bit register is used by the system to perform various control functions on the adapter such as enabling or disabling interrupts.

Bit	Symbol
7	Reset
6 - 2	Reserved = 0
1	DMA Enable
0	Interrupt Enable

Figure 15. Basic Control Register

Bit 7 When this bit is set to 1, the hardware reset signal on the adapter is activated. POS information is not affected.

Bits 6 - 2 Reserved, these bits are always cleared to 0.

Bit 1 When it is set to 1, this bit enables the adapter to present DMA requests to the system. When cleared to 0, this bit disables DMA requests. This bit is optionally cleared to 0 by the adapter upon completion of a data block transfer as indicated by TERMINAL COUNT signal. (See "Programmable Option Select (POS)" on page 9 for more DMA information.)

Bit 0 When it is set to 1, this bit enables the adapter to request an interrupt to the system.

Basic Status Register

This 8-bit register is used by the adapter to present handshaking and other status to the system. System interrupts are disabled prior to reading the Basic Status register.

Bit	Symbol
7	DMA Enable
6	Interrupt Pending
5	Command In Progress
4	Busy
3	Status Out Full
2	Command Interface Register Full
1	Transfer Request
0	Interrupt

Figure 16. Basic Status Register

Bit 7 When it is set to 1, this bit indicates that DMA is currently enabled. When cleared to 0, this bit indicates that DMA is currently disabled. DMA is enabled or disabled by bit 1 in the Command Interface register.

Bit 6 When this bit is set to 1, the adapter is preparing to present an interrupt to the system. Command requests should be held to allow interrupts to be serviced. When this bit is cleared to 0, no interrupts are pending.

Bit 5 When it is set to 1, this bit indicates that one or more commands are in-progress on the adapter. A command is considered to be in-progress from the time the adapter reads the command block until the time the system writes the End-of-Interrupt attention request code to the Attention register.

Bit 4 This bit is set to 1 when the system sends a Command Request attention request code to the Attention register. The system is not permitted to write to the Attention register while this bit is set to 1. This bit is cleared to 0 upon completion of the command block transfer or completion of Abort Command and Reset Adapter attention requests.

Note: When a command block or status block transfer is in progress, interrupts are not presented to the system and bit 4 in this register is set to 1.

Bit 3 When it is set to 1, this bit indicates that a status word is available to be read from the Status Interface register. This bit is cleared to 0 when the Status Interface register is read.

Bit 2 This bit is set to 1, when the system writes a command word to the Command Interface register. This bit is cleared to 0 when the adapter has read it and is ready to accept the next command.

Bit 1 This bit is set to 1, when the adapter is ready for a data transfer operation to occur.

Bit 0 This bit is set to 1, when the adapter is presenting an interrupt to the system. This bit is cleared to 0, when the Interrupt Status register is read by the system.

Note: When a command block or status block transfer is in progress, interrupts are not presented to the system. Bit 4 in the Basic Status register is set during a command block transfer.

Interrupt Status Register

This 8-bit register is used by the adapter to present command completion information at the conclusion of a command.

The system must read this register at the end of an operation for the adapter to reset any existing interrupt request to the system.

Bit	Symbol
7 - 5	Device Select
4	Reserved = 0
3 - 0	Interrupt ID

Figure 17. Interrupt Status Register

Bits 7 - 5 These bits indicate which device completed the command as shown in the following figure:

Bits 7 6 5	Device Selected
0 0 0	Device 0
0 0 1	Device 1
0 1 0	Reserved
0 1 1	Reserved
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Adapter Command

Figure 18. Device Select Codes

Bit 4 Reserved, this bit is always cleared to 0.

Bits 3 - 0 These bits are encoded with a number identifying the source or cause of an interrupt request as shown in Figure 19:

Note: The system can obtain more information about the interrupt by reading the status block from the Status Interface register.

Bits 3 2 1 0	Interrupt
0 0 0 0	Reserved
0 0 0 1	Command Completed with Success
0 0 1 0	Reserved
0 0 1 1	Command Completed with ECC Applied
0 1 0 0	Reserved
0 1 0 1	Command Completed with Retries
0 1 1 0	Format Command Partially Completed, Status Available
0 1 1 1	Command Completed with ECC and Retries
1 0 0 0	Command Completed with Warning
1 0 0 1	Abort Complete
1 0 1 0	Reset Complete
1 0 1 1	Data Transfer Ready - No Status Block
1 1 0 0	Command Completed with Failure
1 1 0 1	DMA Error - The status block corresponding to the command that experienced the DMA error can be read from the Status Interface register. The appropriate error recovery is to retry the entire command.
1 1 1 0	Command Block Error
1 1 1 1	Attention Error

Figure 19. Interrupt Request

Command Interface Register

This 16-bit register transfers a command block from the system to the adapter.

After the system writes a Command Request attention request code and a device select code to the Attention register, it writes the first word from the command block to the Command Interface register. Bit 2 is set to 1 in the Basic Status register when a word is available for the adapter to read. The adapter logic clears bit 2 to 0 in the Basic Status register when the adapter microprocessor reads the Command Interface register. The system may write another word from the command block to the adapter when it detects that bit 2 is cleared to 0 in the Basic Status register.

The adapter causes an interrupt when the command is completed. If the command requires a data transfer step, the adapter interrupts (Data Transfer Ready) when it is ready for the data transfer to take place.

Notes:

1. Do not issue an End-of-Interrupt attention request code in response to a Data Transfer Ready or Attention Error interrupt.
2. There is no status block associated with a Data Transfer Ready interrupt.
3. The status block associated with a DMA Error interrupt is the one corresponding to the command in progress that experienced the DMA Error condition. The adapter cancels the command that got a DMA error before causing the DMA Error interrupt. An appropriate error recovery procedure is for the system to retry the command from the beginning.

In response to receiving an interrupt, the system must read the Interrupt Status register to remove the system interrupt request and determine the source or reason for the interrupt. For other than Data Transfer Ready and Attention Error interrupts, the system reads the Command Complete status block from the Status Interface register.

Status Interface Register

This 16-bit register provides the system with the status block corresponding to a completed command or the current status of a specified device. The system can request a status block for the last command completed by issuing a Read Command Complete Status command to the adapter. The system may also request current status (if a command is not pending) by issuing a Read Device Status Block command.

Status block structure depends on which command was completed. The first word of all status blocks contains the:

- Command number of the completed command
- Device number to which it was addressed
- Number of words to follow in the status block.

The adapter interrupts when a command is complete and the status block is available to be read. After the interrupt occurs, the system polls the Basic Status register to see if bit 3 is set to 1, indicating a status word is available.

If the system is not ready to read any or all words of the status block, it may indicate this by writing the device select code and End-of-Interrupt attention request code to the Attention register. This action terminates processing of the command.

The command complete status for a device is kept by the adapter until another command for that device begins or a Get Current Device Status request is made.

After adapter reset or power-on-reset, the Status Interface register contains the following adapter reset information:

Bit	Description
15 - 8	Word Count
7 - 5	Device Select
4 - 0	Test Error Code

Figure 20. Status Interface Register

Test Error codes are shown in the following figure:

Bits 4 3 2 1 0	Error
0 0 0 0 0	No Error
0 0 0 0 1	Internal RAM Failed
0 0 0 1 0	External RAM Failed
0 0 0 1 1	ROM Failed (checksum)
0 0 1 0 0	Sector Buffer Control Registers Failed
0 0 1 0 1	SERDES RAM Failed
0 0 1 1 0	ECC Registers Failed
0 0 1 1 1	Buffer RAM Failed
0 1 0 0 0	Timer/Interrupts Failed

Figure 21. Test Error Codes

Command Descriptions

The adapter is controlled by the system transferring a command block to the adapter. The command block contains the command number for the function the adapter is to perform and necessary parameters.

The adapter interrupts the system at the completion of a command and presents appropriate interrupt status in the Interrupt Status register. The system can obtain additional information by reading the Get Command Complete status block from the Status Interface register.

The following is an example of the command block structure, which applies for many of the device-related commands:

```
        Command Interface Register Bits
 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0    Remarks

 (Type)( Reserved )       (Device) (  Command  )

 T1 T0  x  x  x  x  1  0  D2 D1 D0 C4 C3 C2 C1 C0   COMMAND

 <------------ Number of Blocks ---------------->

 <---------- Least Significant Word ----------->    RBA

 <----------- Most Significant Word ----------->    RBA
```

Figure 22. Command Block Structure

Bits 15 - 14: These bits are used to specify the length of the command block, including the first word. The lengths are specified as follows:

T1	T0	Length of Command Block
0	0	2 Words
0	1	4 Words
1	0	Reserved
1	1	Reserved

Figure 23. Command Block Length

Bits 13 - 10: Reserved.

Bit 9: This bit is always set to 1.

Bit 8: This bit is always cleared to 0.

Bits 7 - 5: These bits specify the device number for which the command is intended as shown in the following figure:

Bits 7 6 5	Device Selected
0 0 0	Device 0
0 0 1	Device 1
0 1 0	Reserved
0 1 1	Reserved
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Adapter Command

Figure 24. Device Select Codes

Bits 4 - 0: These bits specify the command as shown in the following figure:

Bits 4 3 2 1 0	Command	Uses DMA
0 0 0 0 1	Read Data	Yes
0 0 0 1 0	Write Data	Yes
0 0 0 1 1	Read Verify	No
0 0 1 0 0	Write With Verify	Yes
0 0 1 0 1	Seek	No
0 0 1 1 0	Park Heads	No
0 0 1 1 1	Get Command Complete Status	No
0 1 0 0 0	Get Device Status	No
0 1 0 0 1	Get Device Configuration	No
0 1 0 1 0	Get POS Information	No
0 1 0 1 1	Translate RBA	No
1 0 0 0 0	Reserved	Yes
1 0 0 0 1	Reserved	Yes
1 0 0 1 0	Reserved	No
1 0 1 0 0	Reserved	No
1 0 1 0 1	Get MFG Header	Yes
1 0 1 1 0	Format Unit	Yes
1 0 1 1 1	Format Prepare	No

Figure 25. Adapter Commands

Standard Device Command Blocks

For the following command blocks, the adapter provides a device status block at the conclusion of the command. The reserved word in the commands is ignored by the adapter. Its value is not checked.

Read Commands

Two read commands are supported by the adapter: Read data and Read Verify.

Read Data

This is the normal Read command. The number of blocks specified are read and the data transferred to the system. It supports multiple block operations.

```
       Command Interface Register Bits

15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0  Remarks

(Type)( Reserved )       (Device) (  Command  )

 0  1  x  x  x  x  1  0  D2 D1 D0 0  0  0  0  1  READ DATA

<------------ Number of Blocks ---------------->

<---------- Least Significant Word ----------->  RBA

<----------- Most Significant Word ----------->  RBA
```

Figure 26. Read Data Command Block

Read Verify

This command reads the data from the disk without transferring it to the system. It verifies that the data is readable and that it has the correct ECC code. All read retries including data strobe offset, track offset, and ECC are disabled; soft data errors will therefore appear as hard errors. Positioning retries (recalibrate and re-seek) are enabled.

If the system is using the Read Verify command to verify data immediately after a write, then the proper response to an error on a Read Verify error is one or more Write or Read Verify command retries.

```
        Command Interface Register Bits

15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0  Remarks

(Type)( Reserved )       (Device) (  Command  )

 0  1  x  x  x  1  1  0  D2 D1 D0 0  0  0  1  1  READ VERIFY

<------------ Number of Blocks ---------------->

<---------- Least Significant Word ----------->  RBA

<----------- Most Significant Word ----------->  RBA
```

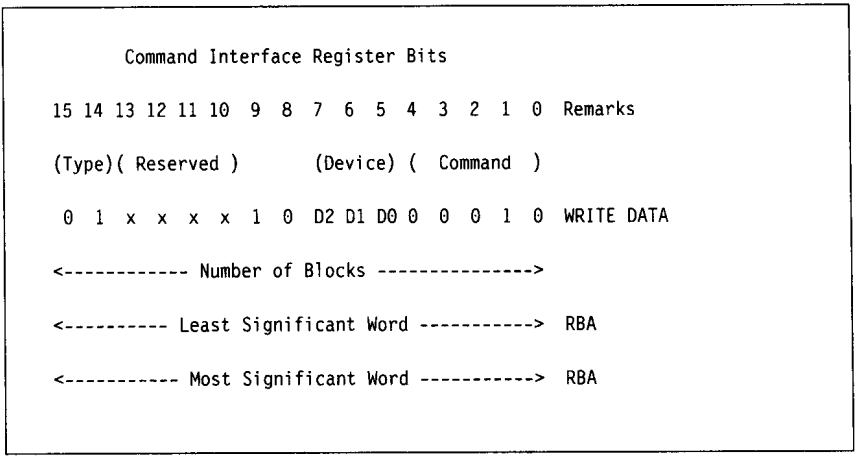
Figure 27. Read Verify Command Block

Write Commands

Two Write commands are supported by this adapter: Write Data and Write With Verify.

Write Data

This is the normal Write command. Data from the system is written on the disk in consecutive blocks. No read-back verify is performed.



Command Interface Register Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Remarks
(Type)		(Reserved)						(Device)			(Command)					
0	1	x	x	x	x	1	0	D2	D1	D0	0	0	0	1	0	WRITE DATA
<---------- Number of Blocks ---------->																
<---------- Least Significant Word ---------->																RBA
<---------- Most Significant Word ---------->																RBA

Figure 28. Write Data Command Block

Write With Verify

This is the same as Write Data, except that a Read Verify is performed after all blocks are written. All read retries including data strobe offset, track offset, and ECC are disabled; soft data errors therefore appear as hard errors. Positioning retries (recalibrate and re-seek) are enabled.

The proper response to an error on a Write With Verify command is one or more Write With Verify command retries.

```
        Command Interface Register Bits

15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0  Remarks

(Type)( Reserved )       (Device) (  Command  )

 0  1  x  x  x  x  1  0  D2 D1 D0 0  0  1  0  0  WRITE VERIFY

<------------ Number of Blocks --------------->

<---------- Least Significant Word ----------->  RBA

<----------- Most Significant Word ----------->  RBA
```

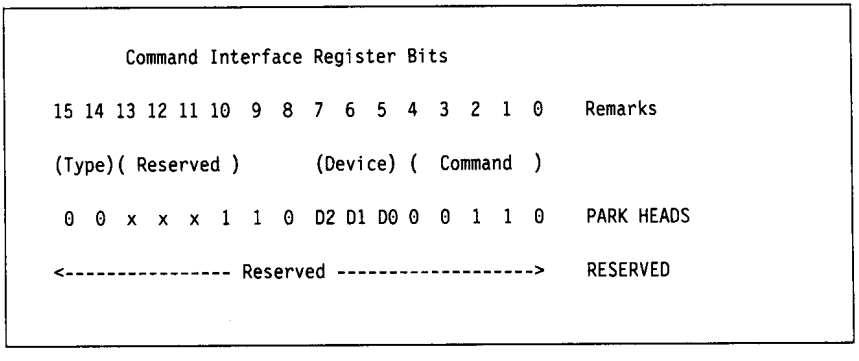
Figure 29. Write With Verify Command Block

Seek Commands

Two seek commands reposition the head on the disk: Park Heads and Seek.

Park Heads

The adapter issues an ESDI Stop Motor command which moves the heads to a safe position to reduce the possibility of damage occurring during physical movement of the devices. After the Park Heads command is complete, commands sent to the adapter will return Device Not Ready until the system has been powered off.



Command Interface Register Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Remarks
(Type)		(Reserved)						(Device)			(Command)					
0	0	x	x	x	1	1	0	D2	D1	D0	0	0	1	1	0	PARK HEADS
<---------- Reserved ---------->																RESERVED

Figure 30. Park Heads Command Block

Seek

This is the normal Seek command, which positions the heads to the proper track for the specified relative byte address (RBA). The adapter provides no verification of final position.

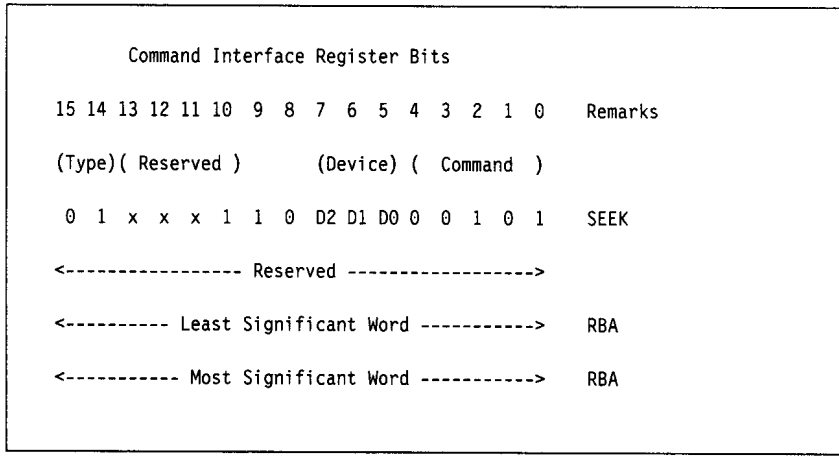


Figure 31. Seek Command Block

Format Commands

Format commands consists of one or two parts. The first part is the actual command which is always used and is transferred using PIO. The second part is the absolute byte address information which is transferred using DMA. Absolute byte address information is only used if the system is specifying defective areas. The Number of Blocks parameter of the command is cleared to 0 if no absolute byte address information is being used, and set to 1 if absolute byte address information is being used. This data is transferred by DMA the same way data is transferred on a write command.

Format Unit

This command causes the adapter to initialize the track formats of the entire disk. All data on the disk prior to the command is destroyed.

```
        Command Interface Register Bits

15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0   Remarks

(Type)                   (Device) (  Command  )

 0  0  0  0  0  1  1  0  D2 D1 D0 1  0  1  1  0   FORMAT UNIT

(      Modifier       )
 0  0  0 PI SA US IS IP  <- Number of Blocks ->
```

Figure 32. Format Unit Command Block

Defect management is provided by the adapter and is controlled by various option bits in the command. These option bits specify the source of the defect information, the desired updating of the defect information and whether extended surface analysis is to be performed.

IP Ignore Primary Defect Map. Primary defect map will not be processed during format.

IS Ignore Secondary Defect Map. Secondary defect map will not be processed during format.

US Update Secondary Defect Map. The secondary map on the disk is updated to reflect the defects found during surface analysis and, those passed with the Format command. If US and IS are both set, the secondary map is replaced.

SA Perform extended surface analysis.

PI Periodic Interrupt option.

Format Unit Periodic Interrupt Option: If the Periodic Interrupt option is not selected when the Format Unit command is used, only one interrupt is issued by the adapter (when formatting is complete).

If the Periodic Interrupt option is used, then many interrupts are issued during the format process. At each intermediate interrupt, the adapter pauses to notify the system of progress through the Status Interface register. Formatting is suspended until the system acknowledges the interrupt and reads the Status Interface register. The system can count these periodic interrupts to allow display of the number of cylinders that have been processed during formatting.

Periodic interrupts are posted as each cylinder completes a phase of the format process. The phase number is available in the Status Interface register when each interrupt is posted. A phase number of 1 indicates that the surface scan phase is in progress. A phase number of 2 indicates that the cylinder format phase is in progress.

Translate Relative Byte Address (RBA)

The system uses this command to translate the relative byte address to the absolute byte address. To deallocate a defective block the system must pass the absolute byte address of that block to the adapter as part of the Format Unit command.

The relative byte address of the block to be deallocated is passed as part of the Translate relative byte address command as shown in the following figure:

Note: When the command completes, a Command Complete status block is available. This Command Complete status block differs from the standard block. The last relative byte address processed value is replaced with the absolute byte address.

The system uses this absolute byte address to construct the list of defects for the Format Unit command.

```
        Command Interface Register Bits

15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0   Remarks

(Type)                    (Device) (  Command  )

 0  0  x  x  x  1  1  0  D2 D1 D0 0  1  0  1  1   TRANSLATE RBA

<----------------- Reserved ------------------>

<---------- Least Significant Word ----------->    RBA

<----------- Most Significant Word ----------->    RBA
```

Figure 33. Translate Relative Byte Address Command Block

Format Prepare

The Format Prepare command is intended as a format interlock to prevent inadvertent data destruction. The Format Prepare command must be issued immediately prior to the Format command. If any other command (to the specified unit) occurs between the Format Prepare command and the Format command, then Format will not occur and the new command terminates with an error.

```
        Command Interface Register Bits

15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0   Remarks

(Type)                    (Device) (  Command  )

 0  0  0  0  0  1  1  0  D2 D1 D0 1  0  1  1  1   FORMAT PREPARE
 0  1  0  1  0  1  0  1  1  0  1  0  1  0  1  0   Hex 55AA
```

Figure 34. Format Prepare Command Block

If this command is not presented immediately before the Format command, the Format command is rejected due to a sequence error.

The adapter ensures proper operation of read, write and ECC mechanisms before formatting.

The contents of the data blocks are shown in the following figure:

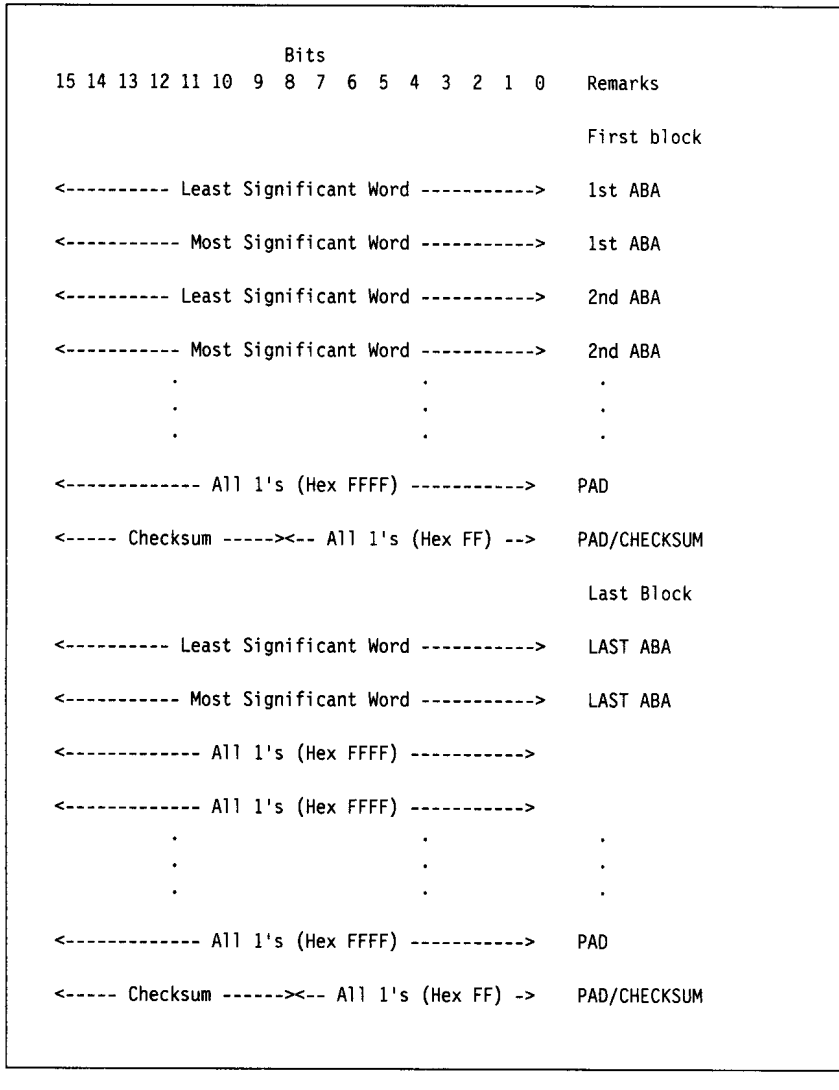


Figure 35. Format Unit Data Block

Absolute byte address information is passed when the system wants to de-allocate bytes that it has identified. The absolute byte address information is a list of the blocks to be de-allocated. The list is in ascending numerical order.

The absolute byte addresses are arranged into 512-byte blocks, and complete blocks are always transferred. All words after the last absolute byte address in a block are filled with 1's; this, along with the block count, can be used to locate the end of the list.

The last 2 words of each block consist of a pad and a checksum. The pad is 3 bytes of all 1's. The checksum is the last byte of the block, and is the twos complement of the sum of the preceding 511 bytes of the block. To verify the block, all 512 bytes of the block are added to generate an 8-bit sum, discarding overflow. If there is no error, the resulting sum is zero.

Note: Words transferred by DMA are arranged low-order byte first. Thus, in Figure 35 on page 33, the 8-bit checksum that appears to the left of the last word of the block is in fact the last byte of the block.

Up to 2 blocks of absolute byte addresses may be transferred, for a total of up to 126 blocks to be deallocated.

The checksum is the 32-bit sum of the 16-bit words that make up the absolute byte address list. In other words, 16-bit words are added to the low-order 16 bits of the checksum and are allowed to accumulate to a 32-bit sum.

The adapter verifies the formatting of each track after write. The device '-index' and '-sector' signals are monitored to ensure proper placement of sectors on the disk. If any errors are noted, reformatting is performed.

When the adapter is instructed to perform extended surface analysis during formatting, it uses the following procedure:

1. Write four different data patterns. The data patterns are repeating patterns (all bytes in the block are the same) with the values of hex 44, hex 22, hex 11, and hex 88.
2. Read 64 times for each write, with retries, offsets, and ECC disabled.

3. Read each write 8 times. If no errors are found it continues with the next step. If errors are found it continues reading until it has tried 64 times.
4. Deallocate the sector if any N of 64 reads indicates an error within four bytes of each other. (N is the "Number of Errors in 64 Reads to Classify Defect" from the manufacturing header of the Primary Defect Map.)

Information Command Blocks

The following information command blocks are supported by the adapter:

Get Device Status

This command requests the adapter to provide the system with the current status of the device selected. The adapter interrupts the system when it has the associated status block available for the system to read.

This command returns the current status of the associated device. The adapter interrupts the system when the status block is available.

```
        Command Interface Register Bits

15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0    Remarks

(Type)                    (Device) (  Command  )

 0  0  x  x  x  1  1  0  D2 D1 D0 0  1  0  0  0    GET DEVICE
                                                    STATUS BLOCK

<---------------- Reserved -------------------->
```

Figure 36. Get Device Status Block

The device status block is shown in the following figure:

```
                Command Interface Register Bits

          15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0  Remarks

          (---- Word Count -----)  (Device) (  Command  )

Word-0     0  0  0  0  1  0  0  1  D2 D1 D0 C4 C3 C2 C1 C0 COMMAND

Word-1    <----- Reserved ------><---- Error Bits------>

Word-2    <----- Device Status --><-- Device Error Code->

Word-3    <----------- ESDI Standard Status ------------>

Word-4    <-------ESDI Vendor Unique Status #1---------->

Word-5    <-------ESDI Vendor Unique Status #2---------->

Word-6    <-------ESDI Vendor Unique Status #3---------->

Word-7    <-------ESDI Vendor Unique Status #4---------->

Word-8    <-------ESDI Vendor Unique Status #5---------->
```

Figure 37. Device Status Block

Word 1 (Bits 15 - 8): Reserved.

Word 1 (Bits 7 - 0): This byte contains the Device Error Code as shown in the following:

Bits 7 - 4 Reserved, these bits are always cleared to 0.

Bit 3 This bit is set to 1 when there was a time out waiting for COMMAND COMPLETE to become active.

Bit 2 This bit is set to 1 when the adapter received a parity error on data being transferred from the attached device.

Bit 1 This bit is set to 1 when there was a time out waiting for TRANSFER ACKNOWLEDGE from the attached device to become inactive.

Bit 0 This bit is set to 1 when there was a time out waiting for TRANSFER ACKNOWLEDGE from the attached device to become active.

Word 2 (Bits 15 - 0) Device Status and Device Error Codes: These codes are shown beginning on page 44.

Word 3 (Bits 15 - 0) ESDI Standard Status: These bits are the ESDI Standard bits. For more ESDI information refer to the Enhanced Small Device Interface Specification[1].

Words 4 - 8 (Bits 15 - 8) ESDI Vendor Unique Status: Attached devices may optionally offer up to 15 "Vendor-unique Status Words" to further define error conditions. The adapter only transfers the first 5 of these status words to the system for review. The adapter does not use these words.

Note: If no words are available, these words are filled with hex 00.

Get Device Configuration

This command requests the adapter to provide device configuration information. The adapter interrupts the system when it has the device configuration status block available. The Get Device Configuration command block is shown in the following figure:

```
        Command Interface Register Bits

15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0    Remarks

(Type)                   (Device) (  Command  )

 0  0  x  x  x  1  1  0  D2 D1 D0 0  1  0  0  1    GET DEVICE
                                                    CONFIGURATION

<---------------- Reserved -------------------->
```

Figure 38. Get Device Configuration Command Block

---

[1] ENDL Consulting, 14426 Black Walnut Court, Saratoga, California 95070.

If the Get Device Configuration command request is to return status for devices 0 or 1, then information about attached devices is returned as shown in the following figure:

```
                    Command Interface Register Bits

             15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0    Remarks

            (------ Word Count ----)  (Device) (  Command  )

Word-0       0  0  0  0  0  1  1  0  D2 D1 D0 C4 C3 C2 C1 C0   GET DEVICE
                                                               CONFIGURATION
Word-1   <---- Spares/Cyl ----->  0  0  0  IS ZD SF FR RT

Word-2   <---------- Least Significant Word ------------>   NUMBER OF

Word-3   <---------- Most Significant Word ------------>     RBA's

Word-4   <------------ Number of Cylinders ------------>

Word-5   <--Sectors per Track-->  <-Tracks per Cylinder->
```

Figure 39. Device Configuration Status Block, Devices 0-1

IS = Invalid Secondary: The first block of the secondary defect map could not be read. The skew amount, push table, and ZD value are not known.

ZD = Zero Defect: When this bit is active, it indicates that there are no defects flagged unusable on the volume.

SF = Skewed Format: When this bit is active, it indicates that the volume was formatted with a sector skewing technique to compensate for devices with extended head switch times.

FR = Removable: When this bit is active, it indicates that the device attached to the adapter has removable media.

RT = Retries: When this bit is active, data and position retries are disabled. When it is inactive, this bit indicates that retries are enabled.

If the Get Device Configuration command request is for device 7, information about the adapter is returned. The Device Configuration Status Block for device 7 is shown in the following figure:

```
                Command Interface Register Bits

          15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0    Remarks

          (---- Word Count -----)  (Device) (  Command  )

Word-0     0  0  0  0  0  1  1  0  D2 D1 D0 C4 C3 C2 C1 C0   GET DEVICE
                                                             CONFIGURATION
Word-1    <--------------- Reserved = 0 ----------------->

Word-1    <----------- Revision Code (LSW) -------------->

Word-1    <----------- Revision Code (MSW) -------------->

Word-1    <--------------- Reserved = 0 ----------------->

Word-1    <--------------- Reserved = 0 ----------------->
```

Figure 40. Device Configuration Status Block, Device 7

The Revision Code in the status block for device 7 is a 32-bit number that identifies the version of adapter microcode.

Get Programmable Option Select (POS) information

This command requests the adapter to provide the system with the contents of the POS registers. The fields that are unknown to the adapter are set to hex FF with the exception of bytes 0 and 1, which are hex FF and hex DD respectively. The adapter interrupts the system when it has the associated status block available for the system to read.

The Get POS Information command block is shown in the following figure:

```
        Command Interface Register Bits

15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0    Remarks

(Type)                    (Device) (  Command  )

 0  0  x  x  x  1  1  0  1  1  1  0  1  0  1  0    GET POS
                                                    INFORMATION

<---------------- Reserved --------------------->   WORD COUNT
```

Figure 41. Get POS Information Command Block

The POS Information status block is shown in the following figure:

```
                Command Interface Register Bits

          15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0    Remarks

         < Adapter ID - POS Regs>  (Device) (  Command  )

Word-0    0  0  0  0  0  1  0  1  1  1  1  C4 C3 C2 C1 C0   GET POS
                                                            INFORMATION
Word-1    1  1  1  1  1  1  1  1  1  1  0  1  1  1  0  1    WORD COUNT

Word-2   <--- POS Register 2 ---><-- POS Register 3 --->

Word-3   <--- POS Register 4 ---><-- POS Register 5 --->

Word-4   <--- POS Register 6 ---><-- POS Register 7 --->
```

Figure 42. POS Information Status Block

Word 0, Bits 15 - 8: This word contains the status block word count.

Word 0, Bits 7 - 0: This field contains the command associated with this status block.

Words 1 - 4: These words contain the contents of the POS Registers.

Note: POS registers 4 - 7. These registers are not used and are filled with hex FF.

Get Manufacturing Header

This command returns the manufacturing (MFG) header, which is contained in the primary defect map, or the entire primary defect map.

If only the manufacturing header is desired, then the system specifies a block count of 1 when using this command. The entire first block of the primary map is returned (of which a portion is the manufacturing header). This block is returned by DMA in the same way as a read command.

If the entire primary map is desired, then the system still begins by specifying a block count of 1. This causes the first block of the primary map to be returned. From this block, the length of the primary map can be determined by examining the "Number of Extension Records" field. To obtain the entire primary map, a second command is issued, specifying the number of extension records plus 1 as the block count. The adapter returns the entire map.

When requesting the entire map, the system must determine the number of blocks in the map using the method outlined above. The adapter does not check to see if the block count exceeds the actual length of the map.

The Get Manufacturing Header command block is shown in the following figure:

```
       Command Interface Register Bits

 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0    Remarks

 (Type)                  (Device) (  Command  )

  0  0  x  x  x  1  1  0  D2 D1 D0 1  0  1  0  1    GET MANUFACTURING
                                                    HEADER
 <----------- Number of Blocks ---------------->
```

Figure 43. Get Manufacturing Header Command

Get Command Complete Status

This command returns the status block associated with the last command executed on the device selected. The status block has the same format and contents as the last command. The adapter interrupts the system when the old status block is available. The interrupt status reflects the conditions after this command, not the previous command, is executed. The command field of the device status block, which is returned as a result of this command, indicates the previous command for which the status pertains. The Get Command Complete Status command block is shown in the following figure:

```
       Command Interface Register Bits

 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0    Remarks

 (Type)                  (Device) (  Command  )

  0  0  x  x  x  1  1  0  D2 D1 D0 0  0  1  1  1    GET COMMAND
                                                    COMPLETE STATUS

 <---------------- Reserved ------------------->
```

Figure 44. Get Command Complete Status Command Block

The Get Command Complete Status status block is shown in the following figure:

```
       Command Interface Register Bits

15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0    Remarks

(Type)                   (Device) (  Command  )

 0  0  0  0  0  1  1  1  D2 D1 D0 0  0  1  1  1    GET COMMAND
                                                    COMPLETE STATUS

<-- Command Status ---> <--- Command Error ---->

<-- Device Status ----> <--- Device Error ----->

<------ Number of Blocks Left to Do ----------->

<-------- Least Significant Word -------------->

<-------- Most Significant Word --------------->

<-Number of Blocks Required for Error Recovery->
```

Figure 45. Get Command Complete Status - Status Block

Word 0 (Bits 15 - 8)

Bit	Description
15 - 8	Status Block Word Count
7 - 0	Contains the command for which this status block was generated.

Figure 46. Word 0

Command/Device Status Codes and Error Codes

Word 1 (Bits 15 - 8) Command Status Code:

Hex Code	Description
00	Reserved
01	Command Completed with Success
02	Reserved
03	Command Completed with Success with ECC Applied
04	Reserved
05	Command Completed with Success with Retries
06	Format Command Partially Complete - Status is Available
07	Command Completed with Success with ECC and Retries
08	Command Completed with Warning (See Command Error Codes)
09	Abort Complete
0A	Reset Complete
0B	Data Transfer Ready - No Status Block.
0C	Command Completed with Failure (See Device Error Codes)
0D	DMA Error - The status block corresponding to the command that experienced the DMA Error can be read from the STATUS INTERFACE. Appropriate error recovery is to redo the entire command.
0E	Command Block Error - A problem occurred in the command block. (See Command Error Codes)
0F	Attention Error - The attention code was bad.
10-FF	Reserved

Figure 47. Command Status Codes

Word 1 (Bits 7 - 0) Command Error Code:

Hex Code	Description
00	No Error
01	Invalid Parameter
02	Reserved
03	Command Not Supported
04	Command Cancelled (By System)
05	Reserved
06	Command Rejected - Adapter Diagnostic Failure
07	Format Rejected - Sequence Error (Requires Format Prepare Command)
08	Format Error - Primary Map Unusable or Defective
09	Format Error - Secondary Map Unusable or Defective
0A	Format Error - Diagnose Failure
0B	Format Warning - Secondary Map Overflow
0C	Format Warning - Non-Zero Defect
0D	Format Error - System Checksum Error
0E	Format Warning - Device Incompatibility
0F	Format Warning - Push Table Overflow
10	Format Warning - More than 15 Pushes in a Cylinder
11	Internal Hardware Error
12	Format Warning - Verify Errors Found
13	Invalid Device for Command
14 - FE	Reserved
FF	Device Error

Figure 48. Command Error Codes

Word 2 (Bits 15-8) Device Error Code:

This applies when the command completed with an error.

Bit	Description
Bit 15	Reserved = 0
Bit 14	Reserved = 0
Bit 13	Reserved = 0
Bit 12	Ready
Bit 11	Selected
Bit 10	Write Fault (Emulated)
Bit 9	Track 0 Flag (Emulated)
Bit 8	Seek or Command Complete

Figure 49. Device Error Codes (Most Significant Bit)

Word 2 (Bits 7 - 0) Device Error Code:

Hex Code	Description
00	No Error
01	Seek Fault (Device Detected)
02	Interface Fault (Parity, Attention, or Command Complete Error)
03	Block Not Found (Could Not Locate ID)
04	AM Not Found (Not Formatted)
05	Data ECC Error (Hard Error)
06	ID ECC Error
07	Relative Byte Address Out of Range
08	Time Out Error
09	Defective Block
0A	Disk Changed
0B	Selection Error
0C	Removable Media Write Protected
0D	Write Fault
0E	Read Fault
0F	No INDEX or SECTOR Pulse
10	Device Not Ready
11	Seek Error (Adapter Detected)
12	Bad Format
13	Volume Overflow
14	No Data AM Found
15	No ID AM and ID ECC Error Occurred (Block Not Found)
16	No Device Configuration Information (Error Reading Information)
17	Missing First and Last RBA Flags
18	No ID's Found on Track
19-80	Reserved
81	Time Out Waiting for SERDES to Stop
82	Time Out Waiting for Data Transfer to End
83	Time Out Waiting for FIFO Request to go Inactive
84	SERDES has Stopped while Waiting for Data Transfer During Format
85	Time Out Waiting for Head Switch
86	Time Out Waiting for DMA Complete
87-FF	Reserved

Figure 50. Device Error Codes (Least Significant Bit)

Word 3 - Number of Blocks Left to Do: This field is used to return the number of blocks for which the command has not completed when an error or cancel stopped the command.

Word 4 - Last Relative Byte Address Processed: Word 4 is the least significant word. This field returns the relative byte address of the last ID processed.

Word 5 - Last Relative Byte Address Processed: This field returns the relative byte address of the last ID processed. Word 5 is the most significant word.

Word 6 - Number of Blocks Requiring Error Recovery: This field returns the number of blocks requiring error recovery due to ECC error or some other cause.

Note: For the commands Park Heads and Seek, words 3 and 6 in the device status block do not apply and are filled with 0's by the adapter.

Adapter Reset

The adapter is reset either by a hardware signal on the channel, a PIO write to the Basic Control register, or by a software command through the Attention register. The software reset is considered a soft reset since the actual hardware reset circuits are not directly activated.

A reset from either source causes the adapter to execute a power-on-reset sequence. The sequence is as follows:

1. Bit 4 in the Basic Status register is set to 1.
2. The adapter internal microcode diagnostics are executed.
3. Results are posted through the Interrupt Status register.
4. The adapter waits for the system to acknowledge by writing an End-of-Interrupt attention request code to the Attention register.
5. Bit 4 in the Basic Status register is cleared to 0.

If the adapter is soft reset immediately following a hardware reset that was completed without an error, the adapter bypasses the on-board diagnostic operation. If a further soft reset is issued, it is processed normally. This is intended to reduce initial program load time required, since a soft reset is always issued at any time the system software is initialized.

Error Recovery

The adapter has the ability to retry certain errors. If the retry is successful, the command continues without system intervention. The Command Complete status block contains information including the number of retries.

If the system must write data to retry an error, it must repeat the DMA transfers.

Read Operations

When reading data, an ID, data field ECC, or other related errors causes the adapter to perform the following error recovery steps:

1. Reread up to four times.
2. Track offset +1, reread two times.
3. Track offset -1, reread two times.
4. Clear track offset to 0 then reread up to four times. If the syndrome is stable for any two consecutive reads, then apply ECC.
5. Data strobe offset +1, reread two times.
6. Data strobe offset -1, reread two times.
7. Restore data strobe offset to 0. Track offset +2, reread two times.
8. Track offset -2, reread two times.
9. Track offset +3, reread two times.
10. Track offset -3, reread two times.
11. Restore track offset to zero. Repeat steps 1 through 10 up to three more times. On the last pass from step 1, if the syndrome is stable for any two consecutive reads, apply ECC.

The adapter uses the Request Configuration Data command to determine if it can use the Track Offset and Data Strobe Offset commands for recovery.

The track and data strobe offsets are cleared to 0 at the conclusion of the error recovery process.

Write Operations

In the event of an ID ECC, or related error such as No Byte Sync, when writing data, the adapter performs a retry up to eight times.

Format Operations

After formatting a track, the adapter verifies the track by reading the ID and data fields. Any errors (other than ECC and No Byte Sync in sectors which have been marked as defective) cause the adapter to retry the format and verify. Up to 2 retries (3 attempts total) can be used. Data strobe offsets, track offsets, and ECC are not used during these retries. If the errors persist, then the format operation is cancelled and an error code is posted to the system.

Positioning Error Recovery

The adapter attempts positioning retries if:

- The adapter receives a Seek Fault indication from the attached device.
- The adapter positively determines that the head is on the wrong track.

Positive identification of the wrong track is made by noting the sector IDs with the Beginning-of-Track and End-of-Track flags set and comparing the target relative byte address to the relative byte address values from those two sectors.

If the sector IDs cannot be read, the data error recovery procedures are invoked until:

- The target ID is found.
- The Beginning- and End-of-Track sectors are read.

This continues until the adapter determines that the target sector is not on the cylinder or until retries are exhausted.

Connectors

The adapter has three adapter-to-device connectors: control (J1) and data (J2 and J3). Power is supplied to the device by a separate power connector.

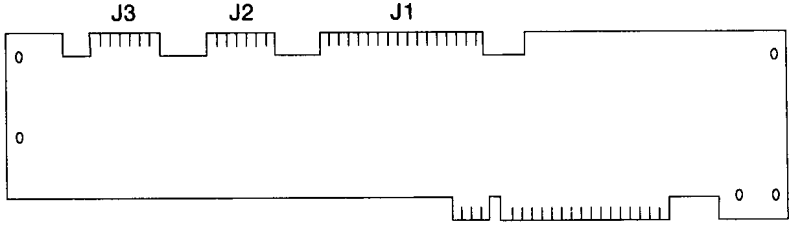


Figure 51. Connectors

Control Connector (J1)

This connector is a 34-pin edge connector that allows connection of multiple devices using a daisy-chained cable.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Ground	2	O	-Head Select 3
3	N/A	Ground	4	O	-Head Select 2
5	N/A	Ground	6	O	-Write Gate
7	N/A	Ground	8	I	-Config/Status Data
9	N/A	Ground	10	I	-Transfer Ack
11	N/A	Ground	12	I	-Attention
13	N/A	Ground	14	O	-Head Select 0
15	N/A	Ground	16	I	-Sector
17	N/A	Ground	18	O	-Head Select 1
19	N/A	Ground	20	I	-Index
21	N/A	Ground	22	I	-Ready
23	N/A	Ground	24	I	-Transfer Request
25	N/A	Ground	26	I	-Device Select 1

Figure 52 (Part 1 of 2). Control Connector (J1)

Pin	I/O	Signal	Pin	I/O	Signal
27	N/A	Ground	28	I	-Device Select 2
29	N/A	Ground	30	I	-Device Select 3
31	N/A	Ground	32	I	-Read Gate
33	N/A	Ground	34	I	-Command Data

Figure 52 (Part 2 of 2). Control Connector (J1)

Data Connectors (J2 and J3)

These connectors are 20-pin edge connectors. One data connector is used for each device in the system.

Pin	I/O	Signal	Pin	I/O	Signal
1	I	-Device Selected	2	I	-Sector
3	I	-Command Complete	4	O	-Address Mark Enable
5	N/A	Reserved	6	O	Ground
7	O	Write Clock	8	O	-Write Clock
9	N/A	Reserved	10	I	Read/Reference Clock
11	I	-Read/Reference Clock	12	N/A	Ground
13	I	NRZ Write Data	14	I	-NRZ Write Data
15	N/A	Ground	16	N/A	Ground
17	I	NRZ Read Data	18	I	-NRZ Read Data
19	N/A	Ground	20	I	-Index

Figure 53. Data Connectors (J2 and J3)

Voltage Requirements

The adapter only uses +5 Vdc.

Notes:

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